2019 General Europractice MPW runs Schedule and Prices

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Dear customer,

Please note that indicated dates are **gds-in deadlines for TSMC, UMC, X-Fab, ON Semiconductor, ams technologies, STMicrolectronics**. If you want to participate onto one of below listed MPW runs, please make sure to do your design registration in time to ensure a seat is reserved for you. How many weeks in advance is mentioned in the notes per foundry. For questions, you can send a mail to:

For TSMC technologies : eptsmc@imec.be
For UMC technologies : epumc@imec.be
For X-fab technologies : epxfab@imec.be
For ON Semiconductor technologies : greta.milczanowska@imec.be
For ams technologies :
If your service center is fraunhofer : virtual-asic@iis.fraunhofer.de
If your service center is CMP : cmp@mycmp.fr
For IHP technologies : virtual-asic@iis.fraunhofer.de
For GLOBALFOUNDRIES technologies : virtual-asic@iis.fraunhofer.de
For STMicrolectronics : cmp@mycmp.fr

ON Semiconductor	J	F	M	A	M	J	J	A	S	O	N	D
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	14		25			3		12		28		
ON Semi 0.7µ C07M-I2T100 100 V - 2M & 3M options	14		25			3		12		28		
ON Semi 0.5µ CMOS EEPROM C5F & C5N – 200 mm			4*									
ON Semi 0.35µ C035U - 4M (3M & 5M optional) only thick top metal	28			15			1		16			2
ON Semi 0.35µ C035 - I3T25U 3.3/25 V 4M (3M & 5M optional) only thick top metal	28			15			1		16			2
ON Semi 0.35µ C035 - I3T80U 80 V 4M - 3M optional (5M on special request)	2			1			8			7		
ON Semi 0.35µ C035 - I3T50U (E) 50 V 4M - 3M optional (5M on special request)			4		27				2			2
ONC18MS (0.18 µm - 1.8/3.3 V - 15V DMOS - 5LM - MiMC - ESD - HiR - EPI)		4		8		10		12		7		9
ONC18MS-LL (=ONC18MS + High Vt)		4		8		10		12		7		9
ONC18HPA (= ONC18MS + DNW + Zener + Stacked MiMC + Native Dev + Schottky)		4		8		10		12		7		9
ONC18-I4T 45/70V HV CMOS (=ONC18MS + 30V + 45V + 70V DMOS)		4		8		10		12		7		9

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.
* ON Semi is experiencing a line load issue for the foreseeable future that pushes out delivery up to 26 weeks

ams	J	F	M	A	M	J	J	A	S	O	N	D
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO		18			13			5			18	
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO					13						18	
ams 0.35µ HV CMOS H35B4D3 120V 4M			5						30			
ams 0.35µ SiGe-BiCMOS S35D4M5/CMOS-RF C35B4M3 4M/4P - MIM			18							14		

Important notes:
- Dates are GDS submission deadlines. The design registration has to be done at least 2 weeks in advance.

Be aware that ams technology will be available only for the coming years. For ongoing projects, Fraunhofer and cmp will provide full support and access for shared engineering run and production. Before starting a new project with ams technologies contact the support team at virtual-asic@iis.fraunhofer.de or cmp@mycmp.fr.

IHP	J	F	M	A	M	J	J	A	S	O	N	D
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	18						26					
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics				12						18		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)					24							
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV		22				14		30				
IHP SG13C SiGe:C CMOS 7M/MIM		22				14		30				
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV		22				14		30				
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE			8									

Important notes:

- Dates are registration deadlines. Final GDSII file must be submitted within 10 days after this date.
- Bumping available for all IHP technologies with extra charge, limited to 200 bumps.
- IHP SG25H4 MPW runs available on request for existing projects only. (Contact: virtual-asic@iis.fraunhofer.de for additional information)

X-FAB	J	F	M	A	M	J	J	A	S	O	N	D
XH018 0.18µ HV NVM CMOS E-FLASH	18			23			29			24		
XT018 0.18µ HV SOI CMOS	4		15			7		23			1	
XS018 0.18µ OPTO		27							11			
XP018 0.18µ NVM CMOS		7				20				10		
XH035 0.35µ HV CMOS	11				3			9			8	
XR013					20						18	

options regular runs	Process modules included for 4 metal option	Process modules included for 6 metal option (5M: XR013)
XH018 0.18µ HV NVM CMOS E-FLASH	LPMOS, MET3, METMID, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO	LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO
XT018 0.18µ HV SOI CMOS	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, METTHK, HWC	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC
XS018 0.18µ OPTO	MOS3LP, MOSLP, METTHIN, MET3, MET4, MRPOLY, ISOMOS, LVTN3D, BCH, MIM23, PPDB, 4TPIX, SFLATPV	MOS3LP, MOSLP, MET3, MET4, MET5, METMID, MRPOLY, ISOMOS, LVTN3D, BCH, MIM23, PPDB, 4TPIX, SFLATPV
XP018 0.18µ NVM CMOS	LP5MOS, MET3, METMID, MRPOLY, HRPOLY, ISOMOS, LVT, MIM, NVM	LP5MOS, MET3, MET4, METMID, METTHK, MRPOLY, HRPOLY, ISOMOS, LVT, MIM, NVM
XH035 0.35µ HV CMOS	MOS, MOS5A, ISOMOS, HVMOSMID, HRPOLY, MIM, METAL4	Not available
XR013 0.13µ RF SOI CMOS	MET1, MET2, MIM, METRB, NOPIMIDE, 2V5DT, HRPOLY, CORE, METBQ	MET1, MET2, METTHKI, MIM, METRB, NOPIMIDE, 2V5DT, IV2DT, LNGI, HRPOLY, CORE, DGOXA, METBQ, LNG2

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 2 weeks in advance.

TSMC	J	F	M	A	M	J	J	A	S	O	N	D
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	30	20	6,27	17,24	8	5,12,26	31	28		2,23	27	
TSMC 0.18 CMOS High Voltage BCD Gen II	9	20,27	27	17	1	5,12	3	7	4	2,30		4
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (8-inch)			13			5		28				4
TSMC 0.13 CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (12-inch)	9	13		10	15		10	14		9	13	
TSMC 90nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power	2			17			10			2		
TSMC 65nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (reserve 4 months in advance)	30	20	27	24	22	26	24	28	25	23	27	
TSMC 40nm CMOS Logic or Mixed-Signal/RF, General Purpose or Low Power (no triple gate oxide)	2	6	6	10	1	5	3	7	4	9	6	4
TSMC 28nm CMOS Logic HPL/HPC/HPC+, RF HPL/HPC/HPC+ (reserve 4 months in advance)		6,27		3	1,29		3,31	28		2,30		4

Important notes:

- Dates are GDS submission deadlines. The design registration has to be done at least 4 weeks in advance unless otherwise specified in above table.
- Contact eptsmc@imec.be if any of the following options are used: MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS

* Dates in red are preliminary and can change after TSMC released the schedule for H2 2019.

STMicroelectronics	J	F	M	A	M	J	J	A	S	O	N	D
ST 28nm CMOS28FDSOI		12								15		
ST 55nm BiCMOS055		12	26					12		22		
ST 65nm CMOS065				29					30			
ST 130nm BiCMOS9MW			4			3					4	
ST 130nm H9SOI-FEM				29					30			
ST 130nm HCMOS9GP			4			3					4	
ST 130nm HCMOS9A											7	
ST 0.16µm BCD8sP			14									
ST 0.16µm BCD8s-SOI		22								2		

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 4 weeks in advance.

UMC	J	F	M	A	M	J	J	A	S	O	N	D
UMC L180 Logic GII, Mixed-Mode/RF		4		29			29			7		
UMC L180 EFLASH Logic GII (1)		25					8				11	
UMC CIS180 Image Sensor – CONV/ULTRA diode (1)				8					30			
UMC L130 Logic/Mixed-Mode/RF		18				24					4	
UMC L110AE Logic/Mixed-Mode/RF			11	22			8		9	28		
UMC L65N Logic/Mixed-Mode/RF - LL	2*		4	1*			1*+22		30*		18	
UMC L65N Logic/Mixed-Mode/RF - SP	2*		4	1*			1*+22				18	
UMC 40N Logic/Mixed-Mode – LP		25		29			1		2		18	
UMC 28N Logic/Mixed-Mode – HPC (1)		11			13			12			11	

options regular runs	Core	IO	MIM	topmetal	special remarks
UMC L180 Logic GII	1.8V	3.3V	1fF	8kA - Max. 1P6M	Redistribution and bumping on request
UMC L180 Mixed-Mode/RF	1.8V	3.3V	1fF	8kA/20kA Max. 1P6M	Redistribution and bumping on request.
UMC L180 EFLASH logic GII	1.8V	3.3V	/	8kA - Max. 2P6M	Please get in touch with imec for the EEFLASH macro information.
UMC CIS18 – CONV	1.8V	3.3V	1fF	5kA – Max.1P4M	Colorfilters and microlenses included
UMC CIS18 – ULTRA	1.8V	3.3V	1fF	5kA – Max.2P4M	Colorfilters and microlenses included. Ultra diode is pinned. PIP capacitor possible.
UMC L130 Logic	1.2V	3.3V	1fF/1.5fF/2fF	8kA Max. 1P8M2T	Two types (out of 3) of devices can be combined: HS,LL, SP. Redistr. to Al.
UMC L130 Mixed-Mode/RF	1.2V	3.3V	1fF/1.5fF/2fF	8kA/20kA Max. 1P8M2T	Two types (out of 3) of devices can be combined: HS,LL, SP. Redistr. to Al.
UMC L110AE Logic/Mixed-Mode/RF	1.2V	1.8V/2.5V/3.3V/5V	1fF/1.5fF/2fF	8kA/12kA/20kA/40kA Max. 1P8M	Metalization is Aluminium. 5V device possible! HS,LL,SP can be combined.
UMC L65N Logic/Mixed-Mode/RF - SP	1.0V, 1.1V	1.8V/2.5V/ 2.5V_OD3.3V/3.3V	2fF	8kA/32.5kA Max. 1P10M	Metallization recommendation on request. Redistribution to Aluminium. * = 32kA topmetal, LVT, MIM in development. 2.5V_OD3.3V not available. ** = 3.3V not available. Please check with us before tapeout.
UMC L65N Logic/Mixed-Mode/RF - LL	1.2V	1.8V/2.5V/ 2.5V_OD3.3V/3.3V	2fF	8kA/32.5kA Max. 1P10M	Metallization recommendation on request. Redistribution to Aluminium. * = 32kA topmetal in development. Please check with us before tapeout.
UMC 40N Logic/Mixed-Mode - LP	0.9V	1.8V/2.5V	2fF	8kA/12kA/32.5kA	Metallization recommendation on request. Redistribution to Aluminium.
UMC 28N Logic/Mixed-Mode - HPC	1.0 & 1.1V	1.8V/2.5V	2fF	8kA/12kA/32.5kA	Metallization recommendation on request. Redistribution to Aluminium.

Important note: Dates are GDS submission deadlines. The design registration has to be done at least 3 weeks in advance.

(1) Contact Europractice when planning to participate to those runs.

GLOBALFOUNDRIES	J	F	M	A	M	J	J	A	S	O	N	D
GLOBALFOUNDRIES 130nm BCDlite	7		11		13		8		9		11	
GLOBALFOUNDRIES 130 nm LP	7		11		13		8		9		11	
GLOBALFOUNDRIES 55 nm LPe		11		15		11		12		14		16
GLOBALFOUNDRIES 55 nm LPx-NVM/LPx-RF		11		15		11		12		14		16
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	2			1			3			1		
GLOBALFOUNDRIES 28 nm SLP/SLP-RF		4			6			5			4	
GLOBALFOUNDRIES 22 nm FDSOI	2		4	29			1		2		4	

Important note: Dates are registration deadlines. Final GDSII file must be submitted within 6 weeks after this date.
* Dates in red are preliminary.

imec	J	F	M	A	M	J	J	A	S	O	N	D
imec Si-Photonics Passives+			27					28				
imec Si-Photonics iSiPP50G		6			22					16		
imec SiN-Photonics BioPIX 300*				1								
imec SiN-Photonics BioPIX 150*§							8					

* imec SiN-Photonics BioPIX: early access runs operated by the H2020-project PIX4Life
*§ imec SiN-Photonics BioPIX 150 MPW run is tentative

CEA-LETI	J	F	M	A	M	J	J	A	S	O	N	D
Silicon Photonic ICs Si310-PHMP2M				2						30		
130nm OxRAM NVM - MAD200						15						

Teledyne Dalsa	J	F	M	A	M	J	J	A	S	O	N	D
Teledyne Dalsa MIDIS	30											

MEMSCAP	J	F	M	A	M	J	J	A	S	O	N	D
PolyMUMPs			26			25			17			16
SOIMUMPs		19			21			21			26	
PiezoMUMPs	15				7			27				

2019 General Europractice MPW runs – Pricelist

Prices are valid for MPW runs starting after 1 January 2019
Accessible for universities, research institutes and companies
Prices and conditions may change at any time without prior notice

STANDARD price : normal price

DISCOUNTED price : only applies to EUROPRACTICE registered (who paid their annual full membership fee) Academic and Research Members from all 28 EU countries and Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, Former Yugoslav Republic of Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine who submit designs for **educational or publicly funded research use only**
Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

Number of prototypes
On Semi: 30 samples
X-FAB: 50 samples
ams: 40 samples
IHP: 40 samples SG25 & SG13, 25 samples using TSV module, PIC & EPIC
UMC: 0.18um, 0.13um, 0.11um: 50 samples
UMC: 65nm: 90 samples
TSMC: 8-inch : 40 samples, 12-inch : 100 samples
imec Si-Photonics passives+: 20 samples, ISIPP50G: 20 samples
miniphotonics: 10 samples, SiN-Photonics BioPIX: 20 samples
imec GaN-IC on SOI: 20 samples
MEMSCAP: 15 samples
GLOBALFOUNDRIES: 50 samples
If you need more prototype samples, please ask for a quotation

Plots
You can order plots/PDF of your designs
- first plot/PDF costs 50 euro
- next plots cost 20 euro each

Packaging : see separate prices and available packages

PRICES IN EURO

ON Semiconductor (formerly AMIS)	STANDARD Price/mm^2	DISCOUNTED Price/mm^2
ON Semi 0.7µ C07M-D 2M/1P	300 [2]	270 [2]
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350 [2]	315 [2]
ON Semi 0.7µ C07M-I2T100 100 V - 2M	525 [1]	485 [1]
ON Semi 0.7µ C07M-I2T100 100 V - 3M	560 [1]	525 [1]
ON Semi 0.5µ CMOS EEPROM C5F & C5N – 200 mm	1150 [2]	1100 [2]
ON Semi 0.35µ C035U 4M (default) including analog options	720 [1]	670 [1]
ON Semi 0.35µ C035U 3M (optional) including analog options	700 [1]	650 [1]
ON Semi 0.35µ C035U 5M (optional) including analog options	800 [1]	750 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 3M	850 [1]	800 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 4M	925 [1]	875 [1]
ON Semi 0.35µ C035 - I3T80U 80 V 5M	1050 [1]	995 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 3M	850 [1]	800 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 4M	925 [1]	875 [1]
ON Semi 0.35µ C035 - I3T50U (or E) 50 V 5M	1050 [1]	995 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 3M (optional)	750 [1]	700 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 4M (default)	770 [1]	720 [1]
ON Semi 0.35µ C035 – I3T25U 3.3/25 V 5M (optional)	800 [1]	750 [1]
ONC18MS 0.18 µm - 1.8/3.3 V - 15V DMOS - 5LM - MiMC - ESD - HiR - EPI	1,100 [1]	1,050 [1]
ONC18MS-LL (=ONC18MS + High Vt)	1,225 [1]	1,195 [1]
ONC18HPA (= ONC18MS + DNW + Zener + Stacked MiMC + Native Dev + Schottky)	1,350 [1]	1,290 [1]
ON 0.18 µm I4T 40/75 V - 5LM – DTI (=ONC18MS + 30V + 45V + 70V DMOS)	1,540 [1]	1,480 [1]

ams	STANDARD Price/mm^2	DISCOUNTED Price/mm^2
ams 0.35µ CMOS C35B4C3 4M/2P/HR/5V IO	640 [12]	580 [12]
ams 0.35µ CMOS C35OPTO 4M/2P/5V IO	800 [3]	700 [3]
ams 0.35µ HV CMOS H35B4D3 120V 4M	880 [3]	800 [3]
ams 0.35µ SiGe-BiCMOS S35D4M5/CMOS-RF C35B4M3 4M/4P - MIM	880 [3]	800 [3]

IHP	STANDARD Price/mm²	DISCOUNTED Price/mm²
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	2500 [7]	2125 [7]
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	3800 [7]	3230 [7]
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics	8000 [7]	6800 [7]
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)	3800 [7]	3230 [7]
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV	6300 [7]	5355 [7]
IHP SG13C SiGe:C CMOS 7M/MIM	4500 [7]	3825 [7]
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV	7300 [7]	6205 [7]
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV	1000 [7]	850 [7]
IHP SPECIAL SERVICES		
bumping (available for all IHP technologies)	One-off fee of 6500 [8]	One-off fee of 6500 [8]
localized back side etching (available for all IHP technologies) not offered for EPIC/PIC runs	One-off fee of 5000 [8]	One-off fee of 4250 [8]
TSV to ground (SG25H4/SG13S)	One-off fee of 5000 [8]	One-off fee of 4250 [8]

X-FAB	STANDARD Price/mm2	DISCOUNTED Price/mm²
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, METMID)	1450 [1, 10]	1380 [1, 10]
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID, METTHK)	1605 [1, 10]	1525 [1, 10]
X-FAB XT018 0.18µ HV SOI CMOS (MET3, METTHK)	1460 [1, 10]	1390 [1, 10]
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	1635 [1, 10]	1555 [1, 10]
X-FAB XS018 0.18µ OPTO (METTHIN, MET3, MET4)	1225 [1, 10]	1165 [1, 10]
X-FAB XS018 0.18µ OPTO (MET3, MET4, MET5, METMID)	1375 [1, 10]	1310 [1, 10]
X-FAB XP018 0.18µ NVM CMOS (MET3, MEDMID)	1260 [1,10]	1200 [1,10]
X-FAB XP018 0.18µ NVM CMOS (MET3, MET4, METMID, METTHK)	1415 [1,10]	1345 [1,10]
X-FAB XH035 0.35µ HV CMOS (MET4)	1035 [1,10]	985 [1,10]

TSMC	STANDARD Price/mm²	DISCOUNTED Price/mm²
All TSMC technologies	Upon request [6]	Upon request [6]

UMC	STANDARD Price/block	DISCOUNTED Price/block
UMC L180 Logic GII, Mixed-Mode/RF	14200 [4]	13500 [4]
UMC L180 CIS 2P4M CONV or 2P4M ULTRA	22700 [4]	21580 [4]
UMC L180 EFLASH Logic GII	18000 [4]	17100 [4]
UMC L130 Logic/Mixed-Mode/RF	23650 [4]	22480 [4]
UMC L110AE Logic/Mixed-Mode/RF	26050 [4]	24760 [4]
UMC L65nm Logic, Mixed-Mode/ RF – LL/SP	37450 [5]	35580 [5]
UMC 40N Logic/Mixed-Mode – LP	72500 [5]	68880 [5]
UMC 28N Logic/ Mixed-Mode – HPC	Upon request, please contact EP	

GLOBALFOUNDRIES	STANDARD Price/mm²	DISCOUNTED Price/mm²
GLOBALFOUNDRIES 130 nm BCDlite	1500 [11]	1400 [11]
GLOBALFOUNDRIES 130 nm LP	1500 [11]	1400 [11]
GLOBALFOUNDRIES 55 nm LPe	4000[11]	3800[11]
GLOBALFOUNDRIES 55 nm LPx-NVM/LPx-RF	4000 [11]	3800 [11]
GLOBALFOUNDRIES 40 nm LP/LP-RF/RF-mmWave	5000 [11]	4700 [11]
GLOBALFOUNDRIES 28 nm SLP-RF	10200 [11]	9700 [11]
GLOBALFOUNDRIES 22 nm FDX FDSOI	14000 [11]	13200 [11]

STMicroelectronics	STANDARD €/mm²	DISCOUNT €/project
ST 28nm CMOS28FDSOI	12000 [18] 24000 + (Area-2) x 9000 [20]	1500
ST 55nm BiCMOS055	7500 [18] 15000 + (Area-2) x 6000 [20]	1200
ST 65nm CMOS065	6000 [19] 30000 + (Area-5) x 4900 [14]	1200
ST 130nm BiCMOS9MW	2900 [19] 14500 + (Area-5) x 2400 [14]	1000
ST 130nm H9SOI-FEM	2200 [19] 11000 + (Area-5) x 1500 [14]	700
ST 130nm HCMOS9GP	2500 [19] 12500 + (Area-5) x 2200 [14]	700
ST 130nm HCMOS9A	2500 [19] 12500 + (Area-5) x 2200 [14]	700
ST 0.16µm BCD8sP	2500 [13] 12500 + (Area-5) x 2200 [14]	1000
ST 0.16µm BCD8s-SOI	2500 [13] 12500 + (Area-5) x 2200 [14]	1000
STMicroelectronics Wafer-Level Bumping	STANDARD €/project	DISCOUNT €/project
wafer 300mm ST 55nm BiCMOS055	25000	1500
wafer 300mm ST 65nm CMOS065	23000	1500
wafer 300mm ST 28nm CMOS28FDSOI	33000	1500

Optional Postprocessing : see pricelist on www.europractice-ic.com

MEMSCAP	STANDARD Price/block	DISCOUNTED Price/block
PolyMUMPs, SOIMUMPs, PiezoMUMPs – 10x10mm	3550	3350

imec Si-Photonics: passives+		Design size	STANDARD price	DISCOUNTED price
Design Size	half block - horizontal	5.15 x 2.5 mm	6100	5800
	half block - vertical	2.5 x 5.15 mm	6100	5800
	1 block	5.15 x 5.15 mm	11600	11000
	2 block - horizontal	10.45 x 5.15 mm	20600	19600
	2 block - vertical	5.15 x 10.45 mm	20600	19600
	Larger sizes		Contact us	
Options	extra set of half block chips (10 samples)		+2000	+2000
	extra set of chips (1 block or larger; 20 samples)		+2000	+2000

- Imec Si-Photonics passives technology is replaced by imec Si-Photonics passives+ technology in 2019. Imec Si-Photonics passives+ allows for metal heaters and edge-couplers, but its introduction also implies a few other changes to the offer. Existing users, please be cautious.
- Number of prototypes in base order: depends on design size: 20 for 1 block or larger, 10 for half block or smaller.
- Due to the nature of MPW logistics, more chips than ordered may sometimes be shipped.

imec Si-Photonics: iSiPP50G		Design size	STANDARD price	DISCOUNTED price
Design Size	quarter block	2.5 x 2.5 mm	10000	9500
	half block - horizontal	5.15 x 2.5 mm	20000	19000
	half block - vertical	2.5 x 5.15 mm	20000	19000
	1 block	5.15 x 5.15 mm	40000	38000
	2 block - horizontal	10.45 x 5.15 mm	80000	76000
	2 block - vertical	5.15 x 10.45 mm	80000	76000
	4 blocks	10.45 x 10.45 mm	150000	142500
	Other		Contact us	
Options	extra set of quarter block chips (10 samples)		+2000	+2000
	extra set of half block chips (10 samples)		+2000	+2000
	extra set of chips (1 block or larger; 20 samples)		+2000	+2000

- Number of prototypes in standard order depends on design size: 20 for 1 block or larger, 10 for half block or smaller.
- Due to the nature of MPW logistics, more chips than ordered may sometimes be shipped.

LETI-CEA OxRAM NVM and Si-Photonic processes - IRT Nanoelec	STANDARD €/mm²	DISCOUNT €/project
130nm OxRAM NVM – MAD200	4000 [13] 20000 + (Area-5) x 3200 [14]	1200
Silicon Photonic Si310-PHMP2M	1600 [15, 16] 16000 + (900/mm²) [15, 17]	700

Teledyne Dalsa (prices only for academia)		STANDARD Price	DISCOUNTED Price
MiDIS	4.0 mm x 4.0 mm	5200	NA

Notes:

1) Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 10 mm²
2) Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 5 mm²
3) Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 7 mm²
4) Price = per block of 5x5mm needed to fit the design in
5) Price = per block of 4x4mm needed to fit the design in
6) Price can be calculated through http://www.europractice-ic.com/TSMC_request_prices.php
   When 4 or more independent sub-designs are submitted in one MPW submission to optimize the minimum charged area, an additional verification charge of 1,000 USD will be applicable. This is regardless of the request and charges for sub die sawing, (5 USD per additional die obtained from the base MPW submission)
7) Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 0.8 mm². The chip area is inclusive of the filler cells outside the sealring
8) Price = per submitted design. For bumping (no size limit, limited to 200 bumps) final wafer thickness for TSV is 75um.
9) Cost for extra services like structures release, subdicing, …
   please refer to http://www.europractice-ic.com/MEMS_pricing.php
10) Area will be rounded upwards to the next mm² (eg. 12.24 mm² will be charged as 13 mm²)
11) Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 9 mm². Any edge length between 1.0 mm to 12.5 mm is possible. The mentioned die size is referred to the Pre-Shrink die size
12) Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 4 mm²
13) Price per mm² for area ≤ 5mm² with minimum charge of 3.43 mm² including seal-ring
14) Price for 5 mm² ≤ Area ≤ 15 mm² including seal-ring. Contact CMP when area is larger
15) Each block is multiple 1 x 2 mm² and/or 2 x 1mm²
16) Price for area ≤ 10 mm² with minimum charge of 2 blocks or 4 mm²
17) Price for additional blocks above 10 mm² with minimum charge of €16.000
18) Price per mm² for area ≤ 2 mm² with minimum charge of 1.25mm² including seal-ring
19) Price per mm² for area ≤ 5 mm² with minimum charge of 1.25mm² including seal-ring
20) Price for 2 mm² ≤ area ≤ 10 mm² including seal-ring. Contact CMP when area is larger than 10 mm²

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