



AMI Semiconductor CMOS C035M-A technology

The 0.35 μ C035M-A technology is a mixed Analogue/Digital process with 5 layer's of metal. It is derived from the fully digital 0.35 μ CMOS process and extended with the following analogue capabilities:

- Precision highly linear thin oxide poly/poly capacitors
- Precision high Ohmic polysilicon resistors

Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for the CMOS 0.35 back-end. A PC based Tanner Design Kit is developed by Europractice. Checks can be performed using the Calibre & Diva decks.

A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.35 μ
Density	15000 gates/sqmm
Core voltage	3.3V
I/O voltages	3.3V
Number of Core cells	393 cells
Number of I/O cells	101 I/O cells
Ram density (single port)	25K bits/mm ²
Poly / Metal layer	2P5M
Substrate / well formation	NON-SELF-ALIGNED N-TUB & P-TUB
Isolation	LOCOS PBL
Gate oxide thickness	7.0 nm
Silicide	Titanium silicide
ILD Planarization	USG/BPTEOS/CMP
IMD Planarization	HDP/PETEOS/CMP
Interconnect	W-plugs filling of stackable contacts and vias
Passivation	Nitride based
Capacitors	Precision highly linear thin oxide poly/poly capacitors
Resistors	Precision high Ohmic polysilicon resistors
Poly pitch	0.9 μ
Metal pitch	1.1 μ for metal 1 1.4 μ for metal 2 to metal 4 2.8 μ for metal 5
Interconnect thickness	0.25 μ for Poly 0.63 μ for metal1 0.72 μ for metal 2 to 4 1.02 μ for metal 5

Key electrical parameters

Parameter @ 3.3V		Typ. Value	Unit
NMOS	VTON (10/0.35, linear extrapolated)	0.59	V
	IDS (10/0.35, Vds=Vgs=3.3V)	530	$\mu\text{A}/\mu\text{m}$
	BVDS (10/0.35, ID=1 μA)	> 7.0	V

Parameter @ 3.3V		Typ. Value	Unit
PMOS	VTON (10/0.35, linear extrapolated)	-0.59	V
	IDS (10/0.35, Vds=Vgs=3.3V)	-245	$\mu\text{A}/\mu\text{m}$
	BVDS (10/0.35, ID=1 μA)	< -7.0	V

Parameter		Typ. Value	Unit
Poly/poly	Cplate	1.1	fF/ μm^2
	Vbd	27	V
HIPO	Rsheet	1000	Ω/sq

Parameter @25 °C		Typ. Value	Unit
Poly1/Poly2 capacitor	Cplate	1.1	fF/ μm^2
	Vbd_max	-	V

Parameter @25 °C		Typ. Value	Unit
High Ohmic poly resistor	Rsheet	1000	Ω/square
P+ unsilicided POLY resistor	Rsheet	120	Ω/square
N+ unsilicided POLY resistor	Rsheet	150	Ω/square

Performance

Speed @3.3V: Unloaded inverter delay of 50ps

Leakage	Typ @ 27C	Max @ 27C	
NMOS (W/L=10/0.35, VDS=3.63V, VGS=0V)	1	20	pA/ μm
PMOS (W/L=10/0.35, VDS=3.63V, VGS=0V)	-1	-20	pA/ μm