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AMI Semiconductor CMOS C035M-D technology

The 0.35µm C035M-D technology is a pure Digital process with 5 layer's of metal available within AMIS Belgium.
Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for the CMOS 0.35 back-end. A PC based Tanner Design Kit is developed by Europractice. Checks can be performed using the Calibre & Diva decks

A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.35µ
Density	15000 gates/sqmm
Core voltage	3.3V
I/O voltages	3.3V
Number of core cells	393 cells
Number of I/O cells	101 cells
Ram density (single port)	25K bits/mm2
Poly / Metal layer	2P5M
Substrate / well formation	Non-Self aligned twin tub
Isolation	LOCOS PBL Isolation
Gate oxide thickness	7.0 nm
Silicide	Titanium salicide
ILD Planarization	USG/BPTEOS/CMP
IMD Planarization	HDP/PETEOS/CMP
Interconnect	W-plugs filling of stackable contacts and vias
Passivation	Nitride based
Poly pitch	0.9µ
Metal pitch	1.1µ for metal 1 1.4µ for metal 2 to metal 4 2.8µ for metal 5

Interconnect thickness	0.25µ for Poly 0.63µ for metal1 0.72µ for metal 2 to 4 1.02µ for metal 5

Key electrical parameters

Parameter @ 3.3V		Typ. Value	Unit
NMOS	VTON (10/0.35, linear extrapolated)	0.59	V
	IDS (10/0.35, Vds=Vgs=3.3V)	530	µA/µm
	BVDS (10/0.35, ID=1µA)	> 7.0	V

Parameter @ 3.3V		Typ. Value	Unit
PMOS	VTON (10/0.35, linear extrapolated)	-0.59	V
	IDS (10/0.35, Vds=Vgs=3.3V)	-245	µA/µm
	BVDS (10/0.35, ID=1µA)	< -7.0	V

Performance

Speed @3.3V: Unloaded invertor delay of 50ps

Leakage	Min @ 27C	Max @ 27C	
NMOS (W/L=10/0.35, VDS=3.63V, VGS=0V)	1	20	pA/µm
PMOS (W/L=10/0.35, VDS=3.63V, VGS=0V)	-1	-20	pA/µm