



AMI Semiconductor CMOS C035U technology

The 0.35 μ C035U-A technology is a mixed Analogue/Digital process with up to 5 layer's of metal. It is derived from the fully digital 0.35 μ CMOS process and extended with the following analogue capabilities:

- Precision highly linear metal/metal capacitors
- Precision high Ohmic polysilicon resistors
- (Floating) medium voltage NDMOS
- Low voltage PNP bipolar transistors
- Low voltage NPN bipolar transistors

Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for the CMOS 0.35 back-end. Checks can be performed using the Calibre deck. A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.35 μ
Density	15000 gates/sqmm (with 5 metal layers)
Core voltage	3.3V, 2.5V, 1.8V or 1.2V (library characterizations)
I/O voltages	3.3V, 2.5V, 1.8V or 1.2V (library characterizations)
Number of Core cells	290 cells (high-speed: amis350uxasca and low-power: amis350uxascb)
Number of I/O cells	101 I/O cells (core-ltd: amis350uxapfa and pad-ltd: amis350uxapta)
Ram density (single port)	25K bits/mm ²
Poly / Metal layer	1P5M
Substrate formation	Nepi on P-substrate
Isolation	LOCOS
Gate oxide thickness	7.0 nm
Metal layers	4 (3 and 5 optional)
Silicide	yes
ILD Planarization	BPTEOS/BPSG/SOG + CMP
IMD Planarization	PETEOS + CMP
Interconnect	W-plugs filling of stackable contacts and vias
Passivation	Nitride based
Capacitors	Precision highly linear metal ² /metal ^{2.5} capacitors Natural metal capacitors
Resistors	Precision high Ohmic polysilicon resistors
Poly pitch	0.85 μ
Metal pitch	1 μ for metal 1 1.1 μ for metal 2 1.1 μ or 1.4 μ for metal 3/4/5 (Depends if Thick top Metal is chosen)

Interconnect thickness	0.30 μm poly/well 1,25 μm metal1/active 0.9 μm metal2/metal1 0.9 μm metal3/metal2 0.9 μm metal4/metal3 0.9 μm metal5/metal4
------------------------	--

Key electrical parameters

Parameter @ 3.3V		Typ. Value	Unit
NMOS	VTON (10/0.35, linear extrapolated)	0.6	V
	IDS (10/0.35, Vds=Vgs=3.3V)	538	$\mu\text{A}/\mu\text{m}$
	BVDSS (10/0.35, ID=1 μA)	> 7.0	V

Parameter @ 3.3V		Typ. Value	Unit
PMOS	VTON (10/0.35, linear extrapolated)	-0.6	V
	IDS (10/0.35, Vds=Vgs=-3.3V)	-250	$\mu\text{A}/\mu\text{m}$
	BVDSS (10/0.35, ID=1 μA)	< -7.0	V

Parameter @ 3.3V		Typ. Value	Unit
LFNDM14	VTON	0.58	V
	IDS (Vds=10V, Vgs=-3.3V)	290	$\mu\text{A}/\mu\text{m}$
	BVDSS (ID=1nA)	>12	V

Vertical Low Voltage PNP		Typ. Value	Unit
Parameter, E_area= 0.64 μm^2	Beta @ Ic= 10 μA	20.1	-
	Bvceo @ Ib0	-33.4	V
	Bvces @ 1 μA	-27.7	V
	Ick	65	μA
Vertical Low Voltage NPN		Typ. Value	Unit
Parameter, E_area= 0.25 μm^2	Beta @ Ic= 10 μA	17.3	-
	Bvceo @ Ib0	20.5	V
	Bvces @ 1 μA	20.9	V
	Ick	4361	μA

Parameter		Typ. Value	Unit
Metal2/Metal2.5	Cplate	1.5	fF/ μm^2
	Vbd	35	V
HIPO	Rsheets	1000	Ω/sq

Technology specification sheet

Parameter @25 °C		Typ. Value	Unit
High Ohmic poly resistor	Rsheel	1000	Ω/square
P+ unsilicided POLY resistor	Rsheel	240	Ω/square
N+ unsilicided POLY resistor	Rsheel	292	Ω/square

Performance

Leakage	Typ @ 27C	Max @ 27C	
NMOS (W/L=10/0.35, VDS=3.3V, VGS=0V)	1	50	pA/μm
PMOS (W/L=10/0.35, VDS= -3.63V, VGS=0V)	-1	-50	pA/μm