



AMI Semiconductor C05M-D technology

The 0.5 μm C05M-D technology is a pure Digital process available from AMIS Belgium foundry. Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for the CMOS 0.5 back-end. A PC based Tanner Design Kit is developed by Europractice. Checks can be performed using the Calibre & Diva decks

A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.5 μm
Density	5000 gates/sqmm
Core voltage	3.3 V, 5.0V optional
I/O voltages	3.3V, 5.0V optional
Number of Core cells	276 cells
Number of I/O cells	155 cells
Poly / Metal layer	2P/3M
Substrate / well formation	Non-Self aligned twin tub N- and P- wells
Isolation	Locos PBL Isolation
Gate oxide thickness (n+ doped)	10.0nm
Silicide	Titanium salicide
ILD Planarization	USG/BPTEOS/CMP
IMD Planarization	Silane-based PECVD + SOG etchback
Interconnect	W-plugs filling of stackable contacts and vias
Passivation	Nitride based
Poly pitch	1.3 μm
Metal pitch	1.6 μm for metal 1 1.9 μm for metal 2 2.5 μm for metal 3
Interconnect thickness	0.3 μm for Poly 0.63 μm for metal1 0.72 μm for metal2 1.02 μm for metal3

Key electrical parameters

Parameter @ 3.3V		Typ. Value	Unit
NMOS	VTON (10/0.5, linear extrapolated)	0.6	V
	IDS (10/0.5, VD=VG=3.3V)	381	$\mu\text{A}/\mu\text{m}$
	Body factor (10/0.5, VD = 0.1V, Vbulk = 0 \rightarrow -2.5V)	0.45	V ^{1/2}
	BVDS (10/0.5, ID=1 μA)	> 7	V

Parameter @ 3.3V		Typ. Value	Unit
PMOS	VTOP (20/0.5, linear extrapolated)	-0.58	V
	IDS (20/0.5, VD=VG=-3.3V)	-166	$\mu\text{A}/\mu\text{m}$
	Body factor (20/0.5, VD = -0.1V, Vbulk = 0 \rightarrow 2.5V)	0.45	V ^{1/2}
	BVP (20/0.5, ID=-1 μA)	< -7	V

Performance

Speed @3.3V Typical delay for unloaded 2 input NAND: 190 ps

Leakage	27C	
NMOS (W/L=10/0.5, VDS=3.63V, VGS=0V)	1	$\text{pA}/\mu\text{m}$
PMOS (W/L=10/0.5, VDS=3.63V, VGS=0V)	1	$\text{pA}/\mu\text{m}$