



AMI Semiconductor C07M-A technology

The 0.7 μm C07M-A technology is a mixed Analog/Digital process available from AMIS Belgium foundry. It is derived from the fully digital 0.7 μm CMOS process and extended with the following analog capabilities:

- Precision highly linear thin oxide poly/dif capacitors
- Precision high ohmic polysilicon resistors
- Low V_t PMOS transistor
- NDMOS transistor
- Bipolar transistor
- Zener zap diode

Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for the CMOS 0.7 back-end. A PC based Tanner Design Kit is developed by Europractice. Checks can be performed using the Dracula & Diva decks.

A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.7 μm
Density	1250 gates/sqmm
Core voltage CMOS 0.7	5.0 V
I/O voltages CMOS 0.7	5.0V
Number of Core cells	126 cells + analog library
Number of I/O cells	108 cells
Poly / Metal layer	1P/2M (optional 3 metals for dedicated runs)
Substrate / well formation	P-sub, self-aligned twin-well
Isolation	Optimised LOCOS
Gate oxide thickness (n+ doped poly gate)	17.0 nm
Interconnect	Aluminium alloy based, low interconnect resistivity
Low V_t	Low V_T PMOS transistors available
Passivation	Nitride based
Capacitors	Precision high linear thin oxide poly/diffusion capacitors
Resistors	Precision high Ohmic polysilicon resistors
Zener zap diode	Non-zapped diode: $V_Z@50\mu\text{A} = 3.5 - 4.2\text{V}$, $R_{diff}@1\text{mA} = 10 - 230 \text{ Ohm}$ Zapped diode: $V_Z@50\mu\text{A} < 0.9\text{V}$, $R_{zapped}@50\mu\text{A} < 20 \text{ KOhm}$
Poly pitch	1.7 μm
Metal pitch	2.2 μm for metal 1 2.8 μm for metal 2
Interconnect thickness	0.42 μm for Poly 0.82 μm for metal1 1.00 μm for metal2

Key electrical parameters

Parameter @ 5.0V		Typ. Value	Unit
NMOS	VTON (20/0.7, linear extrapolated)	0.74	V
	IDS (20/0.7, VD=VG=5V)	358	$\mu\text{A}/\mu\text{m}$
	Body factor (20/0.7, VD=0.1V, Vbulk= 0→6.0V)	0.6	V ^{1/2}
	BVN (20/0.7, ID=1 μA)	7	V

Parameter @ 5.0V		Typ. Value	Unit
PMOS	VTOP (20/0.7, linear extrapolated)	-0.95	V
	IDS (20/0.7, VD=VG=-5.0V)	-176	$\mu\text{A}/\mu\text{m}$
	Body factor (20/0.7, VD=-0.1V, Vbulk=0→-6.0V)	0.42	V ^{1/2}
	BVP (20/0.7, ID=-1 μA)	-7	V

Parameter @ 5.0V		Typ. Value	Unit
PMOS Low Vt	VTOP (20/0.7, linear extrapolated)	-0.78	V
	IDS (20/0.7, VD=VG=-5.0V)	-121	$\mu\text{A}/\mu\text{m}$
	Body factor (20/0.7, VD=-0.1V, Vbulk=0→-6.0V)	0.50	V ^{1/2}
	BVP (20/0.7, ID=-1 μA)	-7	V

Parameter Ae=460 μm^2		Typ. Value	Unit
Bipolar	Hfe	22	-
	BVCEO	30	V
	Vbe	0.566	V

Parameter Lmain= 4.0 μm		Typ. Value	Unit
NDMOS	VT0 (40/4)	0.675	V
	IDS (40/4, VDS=20, VGS=1.5V)	238	$\mu\text{A}/\mu\text{m}$
	IDS (40/4, VDS=20, VGS=5V)	4675	$\mu\text{A}/\mu\text{m}$
	Ron	794	/
	Vbd (max)	40	V
	Vgs (max)	8	V

Parameter @25 °C		Typ. Value	Unit
CAPA capacitor	Cplate	0.75	fF/ μm^2
	Vbd_max	15	V
Parameter @25 °C		Typ. Value	Unit
High Ohmic poly resistor	Rsheet	2000	Ω/square
N-well	Rsheet	1300	Ω/square

Performance

Speed: ring oscillator delay: 170 ps/stage

Leakage	27C	
NMOS (W/L=20/0.7, VDS=7.0V, VGS=0V)	10	pA/ μm
PMOS (W/L=20/0.7, VDS=7.0V, VGS=0V)	10	pA/ μm
LOW Vt PMOS (W/L=20/0.7, VDS=7.0V, VGS=0V)	10	pA/ μm