



## AMI Semiconductor C07M-D technology

The 0.7  $\mu\text{m}$  C07M-D technology is a pure Digital process available from AMIS Belgium foundry. Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for the CMOS 0.7 back-end. A PC based Tanner Design Kit is developed by Europractice. Checks can be performed using the Dracula & Diva decks.

A full set of documentation and design kit is available after the appropriate DKLA is signed.

### Key process technology specifications

Technology	0.7 $\mu\text{m}$
Density	1250 gates/sqmm
Core voltage CMOS 0.7	5.0 V
I/O voltages CMOS 0.7	5.0V
Number of Core cells	126 cells
Number of I/O cells	108 cells
Poly / Metal layer	1P/2M (optional 3 metals for dedicated runs)
Substrate / well formation	P-sub, twin-well
Isolation	Optimised LOCOS
Gate oxide thickness (n+ doped)	17.0 nm
Interconnect	Aluminium alloy based, low interconnect resistivity
Passivation	Nitride based
Poly pitch	1.7 $\mu\text{m}$
Metal pitch	2.2 $\mu\text{m}$ for metal 1 2.8 $\mu\text{m}$ for metal 2
Interconnect thickness	0.42 $\mu\text{m}$ for Poly 0.82 $\mu\text{m}$ for metal1 1.00 $\mu\text{m}$ for metal2

**Key electrical parameters**

Parameter @ 5.0V		Typ. Value	Unit
NMOS	VTON (20/0.7, linear extrapolated)	0.74	V
	IDS (20/0.7, VD=VG=5V)	358	$\mu\text{A}/\mu\text{m}$
	Body factor (20/0.7, VD=0.1V, Vbulk= 0→6.0V)	0.6	V <sup>1/2</sup>
	BVN (20/0.7, ID=1 $\mu\text{A}$ )	7	V

Parameter @ 5.0V		Typ. Value	Unit
PMOS	VTOP (20/0.7, linear extrapolated)	-0.95	V
	IDS (20/0.7, VD=VG=-5.0V)	-176	$\mu\text{A}/\mu\text{m}$
	Body factor (20/0.7, VD=-0.1V, Vbulk=0→-6.0V)	0.42	V <sup>1/2</sup>
	BVP (20/0.7, ID=-1 $\mu\text{A}$ )	-7	V

**Performance**

Speed: ring oscillator delay: 170 ps/stage

Leakage	27C	Unit
NMOS (W/L=20/0.7, VDS=7.0V, VGS=0V)	10	$\text{pA}/\mu\text{m}$
PMOS (W/L=20/0.7, VDS=7.0V, VGS=0V)	10	$\text{pA}/\mu\text{m}$