



## AMI Semiconductor C5F/N - EEPROM technology

The 0.5  $\mu\text{m}$  C5F/N technology is a mixed Analogue/Digital process available from AMIS Pocatello foundry. It is derived from the fully digital 0.5 $\mu\text{m}$  CMOS process and extended with the following analogue capabilities:

- Precision highly linear thin oxide poly2/poly capacitors (PiP)
- Precision high ohmic polysilicon resistors
- 3.3 or 5 Volt operation
- C5N: standard CMOS
- C5F: Thick Gate oxide, optional to C5N
- NASTY cell: No Added Steps Tunneling EEPROM

Europractice distributes the design kit from AMIS, using the Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for CMOS 0.5 back-end.

A full set of documentation and design kit is available after the appropriate DKLA is signed.

### Key process technology specifications

C5N	
Technology	0.5 $\mu\text{m}$
Core voltage	2.5V, 3.3 V, 5.0V
I/O voltages	5.0V
Poly / Metal layer	2P/3M
Substrate / well formation	Self aligned twin tub N- and P- wells
Isolation	Locos Isolation
Gate oxide thickness	13.5 nm (5 V gate/20V drain)
ILD Planarization	BPSG/CMP
IMD Planarization	PECVD
Interconnect	W-plugs filling of stackable contacts and vias
Passivation	Oxide-Nitride based
Capacitors	Precision high linear thin oxide poly/poly capacitors
Resistors	Precision high Ohmic polysilicon resistors
Poly pitch	1.2 $\mu\text{m}$
Metal pitch	1.2 $\mu\text{m}$ for metal 1 1.4 $\mu\text{m}$ for metal 2 1.5 $\mu\text{m}$ for metal 3
Interconnect thickness	0.35 $\mu\text{m}$ for Poly 0.64 $\mu\text{m}$ for metal1 0.57 $\mu\text{m}$ for metal2 0.77 $\mu\text{m}$ for metal3

NASTEE cell (EEPROM)	<p>No Added Steps Tunnelling EEPROM</p> <ul style="list-style-type: none"> <li>❖ Suitable for ID number and coding</li> <li>❖ Programming Voltage: 20V</li> <li>❖ Read @ 3.0 to 5.5 Volts</li> <li>❖ Temperature range: -40 to 125°C</li> <li>❖ Asynchronous Read Mode</li> <li>❖ Reliability <ul style="list-style-type: none"> <li>○ Data retention: &gt;10 years</li> <li>○ Endurance: 100K cycles</li> </ul> </li> <li>❖ Verilog &amp; VHDL Models</li> <li>❖ 2 types <ul style="list-style-type: none"> <li>• Serial EEPROM (parallel 4 to 64 bits) <ul style="list-style-type: none"> <li>○ Erase/Write time: ~10 mS</li> <li>○ Read access time: ~150 nS</li> </ul> </li> <li>• Non-Volatile Latch (organized as parallel 4 to 64 bits) <ul style="list-style-type: none"> <li>○ Erase/Write time: ~10 mS</li> <li>○ Read access time: ~200 nS</li> </ul> </li> </ul> </li> </ul>
<b>C5F</b>	<b>Optional to the C5N technology</b>
Thick Gate extended drain	29.0 nm (15 V gate/20V drain)
Thick Gate nested drain	29.0 nm (12 V gate/20V drain)

**Key electrical parameters of C5N at 5.0 Volts**

Parameter @ 25°C		Typ. Value	Unit
NMOS	VTON (20/0.6, linear extrapolated)	0.696	V
	IDS (20/0.6, VD=VG=5.0V)	450	μA/μm
	Body factor (20/20, VDS = 0.1V, Vbulk = 0→-5V)	0.54	V <sup>1/2</sup>
	BVDS (20/0.6, ID=1μA)	14	V
Parameter @ 25°C		Typ. Value	Unit
PMOS	VTOP (20/0.6, linear extrapolated)	-0.905	V
	IDS (20/0.6, VD=VG=-5.0V)	-260	μA/μm
	Body factor (20/0.6, VD = -0.1V, Vbulk = 0→5V)	0.555	V <sup>1/2</sup>
	BVP (20/0.6, ID=-1μA)	-12	V

**5/20V Extended Drain transistors**

Parameter @ 25°C (max gate voltage = 5 V)		Typ. Value	Unit
NMOS 5/20V	VTON (20/5)	0.75	V
	Vmax=Vbd	28	V
	Ids (20/5, Vds=20, Vgs=5.0V)	2.9	mA
	Leakage	20	pA
Parameter @ 25°C (max gate voltage = 5 V)		Typ. Value	Unit
PMOS 5/20V	VTON (20/5)	-1.1	V
	Vmax=Vbd	-28	V
	Ids (20/5, Vds=20, Vgs=5.0V)	-1.1	mA
	Leakage	-20	pA

Parameter		Typ. Value	Unit
Poly2/poly	Cplate	0.95	fF/μm <sup>2</sup>
HIPO	Rsheets	1000	Ω/sq

**Performance**

Speed @5.0V: inverter delay: 121 ps/stage

Leakage	27C	
NMOS (W/L=20/0.6, VDS=5.5V, VGS=0V)	1	pA/μm
PMOS (W/L=20/0.6, VDS=5.5V, VGS=0V)	-1	pA/μm

**Key electrical parameters at 5.0 Volts of the C5F (extension of C5N)**

## 15/20V Extended Drain transistors

<b>Parameter @ 25°C (max gate voltage = 15 V)</b>		<b>Typ. Value</b>	<b>Unit</b>
NMOS 15/20V	VTON (20/5)	0.95	V
	Vmax=Vbd	28	V
	Ids (20/5, Vds=20, Vgs=5.0V)	8	mA
	Leakage	10	pA
<b>Parameter @ 25°C (max gate voltage = 15 V)</b>		<b>Typ. Value</b>	<b>Unit</b>
PMOS 15/20V	VTON (20/5)	-1.65	V
	Vmax=Vbd	-28	V
	Ids (20/5, Vds=20, Vgs=5.0V)	-2.6	mA
	Leakage	-10	pA

## 12V Double Sided Nested-Drain transistors

<b>Parameter @ 25°C (max gate voltage = 13.2 V)</b>		<b>Typ. Value</b>	<b>Unit</b>
NMOS 12V	VTON (20/5)	0.95	V
	Vmax=Vbd	19	V
	Ids (20/5, Vds=20, Vgs=5.0V)	6	mA
	Body factor (20/20, VDS = 0.1V, Vbulk = 0 → -5V)	1.0	V <sup>1/2</sup>
<b>Parameter @ 25°C (max gate voltage = 13.2 V)</b>		<b>Typ. Value</b>	<b>Unit</b>
PMOS 12V	VTON (20/5)	-1.65	V
	Vmax=Vbd	-14.5	V
	Ids (20/5, Vds=20, Vgs=5.0V)	-2.2	mA
	Body factor (20/20, VDS = 0.1V, Vbulk = 0 → 5V)	1.1	V <sup>1/2</sup>

## 12V Single Sided Nested-Drain transistors

<b>Parameter @ 25°C (max gate voltage = 13.2 V)</b>		<b>Typ. Value</b>	<b>Unit</b>
NMOS 12V	VTON (20/3)	0.95	V
	Vmax=Vbd	19	V
	Ids (20/3, Vds=20, Vgs=5.0V)	9.0	mA
	Leakage	0.5	nA/μm
<b>Parameter @ 25°C (max gate voltage = 13.2 V)</b>		<b>Typ. Value</b>	<b>Unit</b>
PMOS 12V	VTON (20/3)	-1.65	V
	Vmax=Vbd	-14.5	V
	Ids (20/3, Vds=20, Vgs=5.0V)	-2.2	mA
	Leakage	-0.5	nA/μm