



AMI Semiconductor I2T30(E) technology

The Intelligent Interface Technology I2T30 is the medium voltage extension of the AMIS CMOS 0.7 μm mixed signal technology. I2T30 is based on and fully compatible with the C07MA technology and as such incorporates all C07MA rules.

The I2T30 technology as extension of the C07MA comprises:

- Precision highly linear thin oxide poly/diffused capacitors (from C07)
- Precision high ohmic polysilicon resistors (from C07)
- Low V_t PMOS transistor (from C07)
- Non-floating Medium voltage NDMOS: NDMOSC07, NND27D
- Floating medium voltage PDMOS: FPD35D
- Zener zap diode for OTP (from C07)

The I2T30E technology as extension of the I2T30 needs 1 extra mask (PBODY) to generate:

- Floating Medium voltage NDMOS: FND25D
- Floating Medium Voltage NPN: NPN30D
- PBODY resistor

Europpractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for CMOS 0.7 back-end. Checks can be performed using the Dracula decks.

A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.7 μm , refer to the AMI Semiconductor C07M-A technology specification sheet
Technology	I2T30(E)
Core voltage CMOS 0.7	5.0 V
I/O voltages CMOS 0.7	5.0V
Poly / Metal layer	1/2M (optional max. 3 metals for dedicated runs)
Substrate / well formation	P-sub, twin-well
Isolation	LOCOS
Gate oxide thickness (n+ doped)	17.0 nm
Interconnect	Aluminium alloy based, low interconnect resistivity
Low V_t	Low V_T PMOS transistors
Passivation	Nitride based
Capacitors	Precision high linear thin oxide poly/diffusion capacitors
Nwell resistors	1250 Ohms
Resistors	Precision high Ohmic polysilicon resistors
Zener zap diode	Non-zapped diode: $V_Z@50\mu\text{A} = 3.5 - 4.2\text{V}$, $R_{diff}@1\text{mA} = 10 - 230 \text{ Ohm}$ Zapped diode: $V_Z@50\mu\text{A} < 0.9\text{V}$, $R_{zapped}@50\mu\text{A} < 20 \text{ KOhm}$

Poly pitch	1.5µm
Metal pitch	1.8µm for metal 1 2.2µm for metal 2
Interconnect thickness	0.42µm for Poly 0.8µm for metal1 1.0µm for metal2

EEPROM	Optional: 1 extra mask needed (DTUNWIN)
Serial EEPROM	< 128 bits Supply Voltage: 2.7-5.5 Volts Data clock: 5 MHz Operating temperature between -40°C and 150°C Parallel Output
Matrix EEPROM	2048 x 8 bits Supply Voltage: 4.5-5.5 Volts Data clock: 4 MHz Operating temperature between -40°C and 85°C Read/write: 8-bit data bus Address bus: 11 bits

Key electrical parameters

Parameter @ 25°C		Typ. Value	Unit
NMOS	VTON (20/0.7, linear extrapolated)	0.74	V
	Vmax=Vbd	5.5	V
	IDS (20/0.7, VD=VG=5V)	358	µA/µm
	Body factor (20/0.7, VD=0.1V, Vbulk= 0→6.0V)	0.6	V1/2

Parameter @ 25°C		Typ. Value	Unit
PMOS	VTON (20/0.7, linear extrapolated)	-0.95	V
	Vmax=Vbd	5.5	V
	IDS (20/0.7, VD=VG=5V)	-176	µA/µm
	Body factor (20/0.7, VD=0.1V, Vbulk= 0→6.0V)	0.42	V1/2

Parameter @ 25°C		Typ. Value	Unit
Low Vt PMOS	VTON (20/1.2, linear extrapolated)	-0.78	V
	Vmax=Vbd	5.5	V
	IDS (20/1.2, VD=VG=5V)	-121	µA/µm
	Body factor (20/1.2, VD=0.1V, Vbulk= 0→6.0V)	0.5	V1/2

Parameter, floating @ 25°C		Typ. Value	Unit
PDMOS for 30V	VTON	-0.92	V
	Vmax=Vbd	-35	V
FPD35D	Vgsmax (full lifetime)	5.5	V
	Ids (W=40 μm, Vds=20, Vgs=4.0V)	-3320	μA
	Ron*Area	0.228	Ω*mm ²

Parameter, NON-floating @ 25°C		Typ. Value	Unit
NDMOS for 27V	VTON	0.65	V
	Vmax=Vbd	27	V
NND27D	Vgsmax (full lifetime)	5.5	V
	Ids (W=40μm, Vds=20, Vgs=4.0V)	8300	μA
	Ron*Area	0.104	Ω*mm ²

Parameter, @ 25°C		Typ. Value	Unit
PNP	Hfe @ Ic=1 μA	22	-
	BVCEO @ Ic=1 μA	30	V

Parameter @25 °C		Typ. Value	Unit
Poly/Gate Ox/Nwell capacitor	Cplate	0.75	fF/μm ²
	Vbd_max (full life time)	15	V

Parameter @25 °C		Typ. Value	Unit
High Resistance poly	Rsheets	2000	Ω/square
Low Resistance poly	Rsheets	27	Ω/square
N-well	Rsheets (W=20μm, L=80 μm)	1250	Ω/square

I2T30E option, extra PBODY mask

Parameter, floating @ 25°C		Typ. Value	Unit
NDMOS for 25V	VTON	0.95	V
	Vmax=Vbd	25	V
FND25D	Vgsmax (full lifetime)	5.5	V
	I _{ds} (40 μm, V _{ds} =15, V _{gs} =5.0V)	6300	μA
	R _{on} *Area	0.139	Ω*mm ²

Parameter, area= 500 μm ² (unitary device)		Typ. Value	Unit
NPN	H _{fe} @ I _c =10μA	150	-
	B _{vceo} @ I _e =1μA	40	V
	B _{vces}	46	V
	I _{max}	8	mA

Performance

Speed@5.0V: ring oscillator delay: 170ps/stage

Leakage	25C	
NMOS (W/L=20/0.7, V _{ds} =7V, V _{gs} =0V)	< 10	pA/μm
PMOS (W/L=20/0.7, V _{ds} =-7V, V _{gs} =0V)	< 10	pA/μm