



AMI Semiconductor I3T80 technology

The Intelligent Interface Technology (I3T80) is the high voltage extension of the AMIS CMOS 0.35 μm mixed signal technology. I3T80 is an answer to the ever increasing demand for more digital integration in mixed analog/digital ASIC 's and more programmability/flexibility.

It is derived from the fully digital 0.35 μm CMOS process and extended with the following analog capabilities:

- Precision highly linear metal/metal capacitors
- Precision high and dual flavoured medium ohmic polysilicon resistors
- Floating high voltage NDMOS and PDMOS
- (Floating) medium voltage NDMOS
- Floating high voltage and low voltage diodes
- Floating CMOS
- Low voltage PNP bipolar transistors (collector grounded)
- Medium voltage NPN bipolar transistors
- Zener zap diode for OTP
- Buried zener diode for clamping
- Medium voltage floating metal capacitors
- Deep n+ doped guard rings

A single poly gate stack is used.

Existing IP in CMOS 0.35 μm technology from AMIS (C035M) are compatible with this technology.

In future, memory options like Flash and EEPROM matrixes will be available.

Europractice distributes the design kit from AMIS, using the Synopsis & Cadence environment based on the Spectre simulator (Analog Artist) for mixed mode front-end simulation and Silicon Ensemble place&route for CMOS 0.35 back-end. Checks can be performed using the Calibre decks.

A full set of documentation and design kit is available after the appropriate DKLA is signed.

Key process technology specifications

Technology	0.35 μm , refer to the AMI Semiconductor I3T80 technology specification sheet
Technology	I3T80
Density	15000 gates/sqmm (with 5 metal levels)
Core voltage CMOS 0.35	3.3 V
I/O voltages CMOS 0.35	3.3V
Metal layer	4 (5 layers is optional) option with only 3 metal layers is available if no special IP's needed
Substrate / well formation	N-epitaxy on P-sub, retrograde-wells
Isolation	LOCOS
Gate oxide thickness	7.0 nm
ILD Planarization	BPTEOS/BPSG/SOG + CMP
IMD Planarization	PETEOS + CMP
Interconnect	Aluminium alloy based, low interconnect resistivity
Passivation	Nitride based

Capacitors	High linear metal2/metal2.5 capacitors Natural floating metal capacitors
Resistors	Precision high and dual flavoured medium ohmic polysilicon resistors Unsalicided N+ and P+ resistors N-well and P-well diffused resistors
Poly pitch	0.9 μm
Metal pitch	1.1 μm for metal 1 1.4 μm for metal 2,3,4 2.8 μm for metal 5
Interconnect thickness	0.31 μm poly/well 1,25 μm metal1/active 0.73 μm metal1/poly 0.8 μm metal2/metal1, metal3/metal2, metal4/metal3, metal5/metal4

Key electrical parameters

NMOS Transistor		Typ. Value	Unit
Parameter @ 25°C	VTON (10/0.35, linear extrapolated)	0.59	V
	Vmax=Vbd	3.6	V
	IDS (10/0.35, Vds=Vgs=3.3V)	530	$\mu\text{A}/\mu\text{m}$
PMOS transistor		Typ. Value	Unit
Parameter @ 25°C	VTON (10/0.35, linear extrapolated)	-0.57	V
	Vmax=Vbd	-3.6	V
	IDS (10/0.35, Vds=Vgs=3.3V)	-250	$\mu\text{A}/\mu\text{m}$
Floating NMOS @ 80V		Typ. Value	Unit
Parameter @ 25°C	VTON (10/0.35, linear extrapolated)	0.59	V
	Vmax=Vfloat to Psubtrate	80	V
	Vmax=Vbd	3.6	V
	IDS (10/0.35, Vds=Vgs=3.3V)	530	$\mu\text{A}/\mu\text{m}$
Floating PMOS @ 80V		Typ. Value	Unit
Parameter @ 25°C	VTOP (10/0.35, linear extrapolated)	-0.57	V
	Vmax= Vfloat to Psubtrate	80	V
	Vmax=Vbd	-3.6	V
	IDS (10/0.35, Vds=Vgs=-3.3V)	-250	$\mu\text{A}/\mu\text{m}$

Floating NDMOS for switching application: VFNDM80		Typ. Value	Unit
Parameter @ 25°C	VTON	0.54	V
	Vmax=Vbd	70	V
	Vgsmax (full lifetime)	3.6	V
	Ids (Vds=40, Vgs=1.5V)	100	$\mu\text{A}/\mu\text{m}$
	Ron*Area (With isolation)	0.26	$\Omega^*\text{mm}^2$
Floating NDMOS for analog application: VFNDM80A		Typ. Value	Unit
Parameter @ 25°C	VTON	0.56	V
	Vmax=Vbd	70	V
	Vgsmax (full lifetime)	3.6	V

Technology specification sheet

	Ids (Vds=20, Vgs=3.3V)	10.5	mA
	Ron*Area (With isolation)	0.325	Ω *mm ²
Floating medium voltage NDMOS		Typ. Value	Unit
Parameter @ 25°C	VTON	0.58	V
	Vmax=Vbd	14	V
	Vgsmax (full lifetime)	3.6	V
	Ids (Vds=10, Vgs=3.3V)	300	μ A/ μ m
	Ron*Area	0.031	Ω *mm ²
Floating PDMOS: LFPDM80		Typ. Value	Unit
Parameter @ 25°C	VTON	-0.56	V
	Vmax=Vbd	-70	V
	Vgsmax (full lifetime)	-3.6	V
	Ids (Vds=-40, Vgs=-1.5V)	18.5	μ A/ μ m
	Ron*Area	0.28	Ω *mm ²

Vertical Low Voltage PNP: VPB		Typ. Value	Unit
Parameter, E_area= 0.64 μ m ²	Hfe @ Ic= 10 μ A	8	-
	Bvceo @ Ic=1 μ A	-63	V
	Bvces @ Ic = 1 μ A	-67	V
	Icmax	250	μ A
Vertical Low Voltage "High gain" PNP transistor: VPHB		Typ. Value	Unit
Parameter, E_area= 0.64 μ m ²	Hfe @ Ic= 100 nA	115	-
	Bvceo @ Ic=1 μ A	> 80	V
	Bvces @ Ic = 1 μ A	> 100	V
	Icmax	250	μ A

Zener diode: PBZD		Typ. Value	Unit
Parameter, W=2 μ m	Vz @ 100 μ A	4.6	V
	Rzener	45	Ω
	Ileak @ Vz=0.5V	200	nA
Zapping Zener diode for OTP: UZZD		Typ. Value	Unit
Parameter, W=2 μ m	Vz @ 1 μ A	1.5	V
	Vbd @ 10 mA	4.5	V
	Ileak_max @ 1V	1.4	mA
Floating High Voltage diode: FID80		Typ. Value	Unit
Parameter, K_area= 6.76 μ m ²	Vak_reverse, Ia=-100nA	> 80	V
	Vak_forw, Ik=1 μ A	0.79	V
	Isub/IA, Va=0.7V	0.5	%
Poly diode for gate clamping: POLYD		Typ. Value	Unit
Parameter, W=6 μ m	Vreverse @ Ia=10 μ A	6.8	V
	Ileak/W @ Vrev=3.6V	< 20	nA/ μ m

Metal2/metal2.5 Capacitor: MIMC		Typ. Value	Unit
Parameter @ 25°C	Cplate	1.5	fF/ μ m ²
	Vbd_max (full lifetime)	3.6	V

Resistors		Typ. Value	Unit
Parameter @ 25°C	High Resistance Poly: HIPO	975	Ω/square
	Unsalicide P+ Poly: PPOLR	240	Ω/square
	Unsalicide N+ Poly: NPOLR	292	Ω/square

Performance

Speed @3.3V: Unloaded inverter delay of 50ps

Leakage	25°C	
NMOS (W/L=10/0.35, Vds=3.63V, Vgs=0V)	1	pA/μm
PMOS (W/L=10/0.35, Vds=-3.63V, Vgs=0V)	-1	pA/μm