

EUROPRACTICE Design Contest
UMC 90nm technology
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Design Contest Winning Design

A 1.5 GHz Phase-Locked Loop

By

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Certified for free fabrication by
EUROPRACTICE on a *mini@sic* run

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Presented phase-locked loop is one of steps taken towards creating a fully integrated GPS/Galileo receiver in the VLSI Engineering and Design Automation Division of Warsaw University of Technology. During design special attention was paid to minimize influence of process, temperature and supply voltage variations on the phase-locked loop parameters.

The key to achieve the specifications was proper design of RF circuits, especially the voltage controlled oscillator, in which a high-Q inductor and varactors, available in UMC 90 nm technology, were used.

| Parameter | Specification |
|--------------------------------|---|
| Output frequency | 1.571328 GHz |
| Output Signal | Quadrature and differential |
| Supply voltage | 1.2 V \pm 10 % |
| Temperature variation | -40 °C – 125 °C |
| Power consumption | <4 mW |
| Phase noise | <-85 dBc/Hz in-band <-144 dBc/Hz @ 132 MHz |
| Tolerance to process variation | All process corners |
| DRC rules | DFM-5 |

