



austriamicrosystems 0.35 μ m SiGe-BiCMOS (S35)

Description

austriamicrosystems 0.35m SiGe-BiCMOS process is based on the proven 0.35m mixed-signal CMOS process and includes an additional high performance analog oriented SiGe HBT transistor module. This advanced RF-process offers high-speed HBT-transistors with excellent analog performance such as high f_{max} and low noise as well as complementary MOS transistors with the option of 5V I/O CMOS transistors. Accurately modeled high linear precision capacitors are available as Poly1 / Poly2 or Metal2 / Metal3 versions. The modular integration of linear resistors, high quality varactors and thick Metal 4 spiral inductors makes this process ideally suitable for a wide range of high performance RF applications up to 20 Gb/s.

Applications

GSM, DCS1800, PCS1900, IS95, UMTS Front-end
 DECT, PHS, Bluetooth, Home-RF Front-end
 ISM Receivers, Transmitters and Transceivers for: 868MHz, 915MHz, 2.4GHz, 5.6GHz
 GPS, Glonass
 Wireless LAN, Hyper LAN up to 5.6 GHz
 ATM, Sonet, Fibre Channel Transceivers up to 10-20Gb/s
 Satellite Direct Receivers
 Clock recovery circuits up to 10 GHz

Key Features

S35D4M5 4P/4M SiGe BiCMOS Mixed Signal, RF, PIP+MIM, thick metal, HR poly, 5V periphery
 Feature Sizes: 0.35m gates / 0.40m emitters
 Supply Voltage: CMOS 3.3V; periphery up to 5.5V
 $f_t > 60$ GHz, $f_{max} > 70$ GHz
 $V_{ceo} > 2V$

Design Kits

CADENCE Design Framework II

Device Library (pcells)
 Spectre Simulation Models
 CMOS Core and Peripheral Cell Libraries
 RF-Peripheral Cells
 Spiral Inductors
 Accurate Package Models
 Dynamic Link to Agilent ADS and RFDE

Agilent - Advanced Design System

Device Library
 RF-Peripheral Cells
 Spiral Inductors
 Accurate Package Models
 IFF Schematic Transfer to/from Cadence
 ADSSim Simulation Models

Simulation Parameters for: ELDO, HSPICE, SMASH, SPECTRE, ADS, SMARTSPICE