



austriamicrosystems 0.35 μm CMOS Opto (C35B401)

Description

austriamicrosystems' 0.35 μm CMOS Opto process offers high sensitivity at low dark current. Only one additional inorganic ARC layer is required on top of the CMOS base process, making this a high performance low cost solution.

An 14 μm EPI substrate is offered for further performance enhancements. All options of the advanced 0,35 μm mixed-signal polycide-gate CMOS process include up to 4 levels of metal, a full set of capacitors and resistors are available providing high performance digital and analog capabilities.

The high density CMOS standard cell library is optimized for synthesis and 3- and 4-layer routing guarantees highest gate densities. Peripheral cell libraries are available for 3.3V and 5V with high driving capabilities and excellent ESD performance.

Qualified digital macro blocks (SPRAM, DPRAM, and diffusion programmable ROM) are available on request. A variety of high performance analog-to-digital and digital-to-analog converters can be provided for integration on the same ASIC.

Key Features

The CMOS Opto process option provides enhanced optical sensitivity for embedded photodiodes and high density CMOS camera products.

- High sensitivity low dark current 0,35 μm CMOS Opto process
- Low cost – only 1 additional process step (Inorganic ARC Layer)
- Customer-specific wavelength optimized ARC layer based on electrical and optical simulations possible
- 14 μm EPI substrate (20 μm EPI substrate optional)
- All features of advanced mixed signal 0.35 μm CMOS available
 - 3 to 4 metal layers
 - Poly Insulator Poly and Metal Insulator Metal Caps
 - 3.3V/5V Digital Logic

Photo Diode X-section

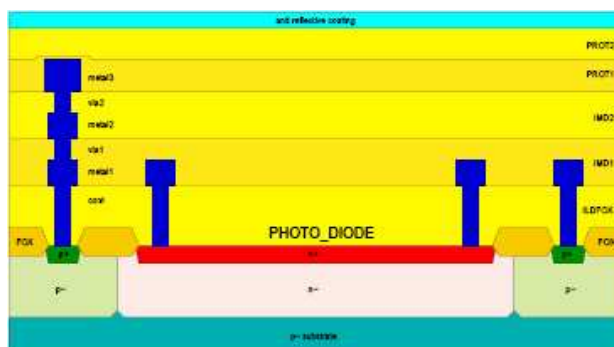


Photo Diode Key Features (for 14 μm EPI)

Responsivity of Photodiode@850nm	330 mA/W
Responsivity of Photodiode@550nm	290 mA/W
Cut-Off Frequency of Photodiode	>20 MHz
Dark Current of Photodiode	<45 pA/cm ²(at 27 °C)
	<40 nA/mm ²(at 125 °C)
Temp. Coeff. of Responsivity@670nm	0.02 %/K
Temp. Coeff. of Responsivity@870nm	0.4 %/K
minimum Pixel size	6µm x 6µm
Cap per area for Photodiode	0.08 fF/µm ²

Design Kits

We offer a unique design environment known as the HIT-Kit (High Performance interface Tool-Kit).

It provides all the building blocks required to create complex Mixed-Signal designs using our specialized processes. The HIT-Kit is based on state-of-the-art software from all major CAD companies.

SPICE modeling

The accuracy of the device models results in shorter design cycles, superior product quality and accelerated time to market throughout the entire "supplychain".

We make accurate measurements of active and passive devices and extract model parameters based on state-of-the art electrical models for exact prediction of MS/analog and high voltage circuit performance. SPICE simulator tools MS/Analog and RF simulator libraries for Spectre, Eldo, ADS, HSPICE, and SmartSpice are supported.

Verification tools

We support Interactive verification with Assura (Cadence) and Calibre (Mentor Graphics) and full chip verification.

- Extraction concept allows support of a myriad of devices.
- Parasitic diodes and capacitances with charge sharing.
- Selective RC extraction.
- Substrate extraction with SubstrateStorm.
- Split substrate for mixed signal simulation of layout.
- Automatic planarity improvements on GDSII data.
- Automatic generation of slots in Metal power busses.