

# OPEN COURSE PROGRAM

## ADVANCED PACKAGING

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Payment has to be done by bank transfer upon receipt of the invoice.

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OPEN COURSE PROGRAM  
IMEC ACADEMY



# OPEN COURSE PROGRAM

## ADVANCED PACKAGING

October 5<sup>th</sup> 2011 - October 6<sup>th</sup> 2011

### COURSE ABSTRACT

This course will address advanced packaging and assembly technologies. These are strongly driven by the rapid evolution of microelectronics and the increasing complexity of electronic systems. Novel technology trends will be discussed. These have a strong impact on the way electronic systems are designed and manufactured. Electronic packaging is a highly multidisciplinary field, where electrical engineering, mechanical engineering and material science play a key role.

### TARGET AUDIENCE

In this course various aspects of the relation between RF design and RF system integration technology will be thoroughly discussed. On one hand this course will be particularly interesting for RF designers, e.g. RF IC designers and PCB designers, who are increasingly faced with design issues in novel packaging and interconnection technologies, particularly RF SiP applications. On the other hand, technology engineers involved in the fabrication of such parts and systems may benefit from the course by getting a better understanding of the strong link between RF design and RF technology. The course is intended to give a basic understanding of on-chip and SiP integrated passive devices in various technologies and to guide you through the variety of technologies available. Focus will be on on-chip and off-chip passive components, circuit design and antenna integration.

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## PROGRAM

Wednesday October 5<sup>th</sup> 2011

### ▶ 13h00-13h40

#### **IC packaging** (Eric Beyne, imec Belgium)

Demands for increased miniaturization and performance of electronic systems have driven traditional IC packaging technologies to higher levels of sophistication and miniaturization. In this session, the different styles of IC packages and their evolution will be discussed, from through-hole to surface mount, from leaded to leadless packages and from 2D to 3D packaging.

### ▶ 13h40-14h20

#### **Wafer level packaging** (Eric Beyne, imec Belgium)

The ultimate miniaturized package has a size equal to the die size. Such packages may be fabricated at the wafer level, before die singulation. This not only results in the smallest possible packages, but also enables cost reduction. All die on a wafer are simultaneously packaged, in contrast to the sequential traditional package flows. This session will focus on technologies such as flip chip bumping, redistribution and wafer level CSP. Also possibilities for 3D-WLP technologies will be discussed.

### ▶ 14h20-15h10

#### **Printed circuit board and flexprint technology** (Johan De Baets, imec Belgium)

The latest developments in printed circuit board and flexprint technology will be highlighted. For the rigid board technology the focus will be on sequential build-up and micro via technology, and on embedded components (passive and active). New technologies with very thin flexible circuits and stretchable electronic circuits, including embedded components, will be shown, with emphasis on applications in lightweight, wearable

electronic systems.

### ▶ 15h30-16h30

#### **Thermal management** (Herman Oprins, imec Belgium)

After introducing the main trends in thermal management for IC packages in electronic systems, the basics of thermal heat transport by conduction, convection and radiation will be briefly explained. The session elaborates on the method of using thermal resistance/impedances for packages and systems characterization, assisted by several practical examples. Also an overview of methods for temperature measuring of IC packages will be given. The session ends with an overview of methods for passive/active cooling of electronic systems.

### ▶ 16h30-17h30

#### **Solder reliability issues on package and on board level** (Riet Labie, imec Belgium)

This session starts with an overview of possible packaging induced IC failure modes, package failure modes, and interconnect failure modes. This includes both well known failure modes such as 'the pop-corn effect', and less known issues such as 'brittle fracture at low temperatures'. The main failure mechanisms will be explained in more detail. Next several reliability test methods will be described, including testing according to well-known standards, and testing using a failure driven test methodology. Also some techniques that can be used for failure analysis of the packages will be described.

Thursday October 6<sup>th</sup> 2011

### ▶ 8h30-9h30

#### **Reliability analysis using thermal simulation** (Bart Vandeveld, imec Belgium)

The scope of this course is how to estimate by

Finite Element Modelling based simulation, the maximum temperature increase inside a chip package due to uniform heating in the active area of the chip and by joule heating in the wire bond or solder interconnects, typical for high current applications. Additionally, a methodology is shown how to extract correct material properties from transient thermal measurements.

### ▶ 9h30-10h30

#### **Reliability analysis using mechanical simulation** (Mario Gonzalez, imec Belgium)

Abstract TBD

### ▶ 10h50-11h50

#### **Board level assembly technology** (Geert Willems, imec Belgium)

The basics of electronic assembly technology will be explained. The session will focus on lead-free soldering being the interconnection methodology most widely used in the electronics industry. The goal of the session is to provide a basic understanding of the different assembly processes used in industrial electronic assembly and the related boundary conditions.

### ▶ 12h40-13h40

#### **Design for manufacturing: how to make a product out of an electric schematic** (Geert Willems, imec Belgium)

An electronic product is a physical entity that must fulfill a multitude of requirements besides performing the functionality that it has been designed for. These requirements are related to its dimensions, weight, appearance, cost, quality, reliability, reparability, environmental impact, ability to recycle, etc. Based on the electronics assembly session the importance of Design-for-Manufacturing as a mandatory practice to achieve high quality, reliable electronic products at low manufacturing costs will be explained.

### ▶ 13h40-14h40 + 15h00-16h00

#### **EMC and signal integrity** (Luc Martens, Ghent University)

As bandwidths of signals increase, parasitics and transmission line effects of boards and packages influence significantly the signal quality. At the same time, the passive interconnections become more vulnerable to external interference. Switching noise and ground bounce effect will also play a role in the signal integrity. The concepts of Electromagnetic Compatibility and signal integrity will be explained and illustrated. Rules of thumb for good EMC design will be presented.

## COURSE LOCATION

The course will take place at imec, Leuven. Imec is the largest independent microelectronics R&D center in Europe, with an annual budget over 300 million euro and a staff of over 1470 people. R&D ranges from design of complex single-chip and single package systems for telecommunications and multimedia, over new process technologies (18nm node) to non-volatile memories, optoelectronics, photo-voltaics, area-array packaging, etc.

Route description: <http://bit.ly/g4OSrO>

## FEES AND REGULATIONS

The participation fee is 600 EUR, excl. 21% VAT.

Flemish academic staff can participate for free. Flemish companies should contact the training office ([training@imec.be](mailto:training@imec.be)) for special conditions.